Prototype 2 wafers measurements at
Univ. of New Mexico

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ATLAS Pixel Sensor Meeting
Feb 05, 2000.

Outline

• Breakdown Voltages

• Quality Yields

• Currents

• Summary
The layout of sensors on the wafer. The sensors are numbered counter-clockwise and spiral-wise starting from TIIad - number 0.
The distribution of the breakdown voltages over the sensors. The sensors (at the picture “chips”) are given the numbered in a “spiral” way (see the illustrating picture). The breakdown voltages are determined according to QA procedure.
The distribution of the breakdown voltages for tiles and tile-like single-chips for CiS batches. The difference of Tiles and Single-chips with smd topology is obvious.
The distribution of the breakdown voltages for tiles and tile-like single-chips for IRST batches.

⇒ The distributions lack a statistics unfortunately -
The quality flags defined according to QA. The breakdown voltages defining the quality are 40V and 150V.
The percentage of CiS and IRST sensors for various quality flags.

- $Qfl = -1$ - 'bad' sensor, $V_{bd} < 40V$
- $Qfl = 0$ - 'medium' sensor, $40V < V_{bd} < 150V$
- $Qfl = +1$ - 'good' sensor, $150V < V_{bd}$
The percentage of CiS and IRST sensors with 'small dot' bias grid for various quality flags.

- Qfl=-1 - 'bad' sensor, $V_{bd} < 40V$
- Qfl=0 - 'medium' sensor, $40V < V_{bd} < 150V$
- Qfl=+1 - 'good' sensor, $150V < V_{bd}$
The yields of sensors with quality flag +1, 'good' ones:

<table>
<thead>
<tr>
<th>vendor</th>
<th>any sensor</th>
<th>Tiles</th>
<th>tile-chips</th>
<th>TIsmd</th>
<th>STsmd</th>
</tr>
</thead>
<tbody>
<tr>
<td>CiS</td>
<td>77%</td>
<td>53%</td>
<td>72%</td>
<td>75%</td>
<td>100%</td>
</tr>
<tr>
<td>IRST</td>
<td>35%</td>
<td>6%</td>
<td>60%</td>
<td>17%</td>
<td>50%</td>
</tr>
</tbody>
</table>

⇒ $(0.75)^{1/16} = 0.98$

⇒ $(0.17)^{1/16} = 0.895$

The yields of sensors with quality flag 0 or +1, that is 'medium' and 'good' ones:

<table>
<thead>
<tr>
<th>vendor</th>
<th>any sensor</th>
<th>Tiles</th>
<th>tile-chips</th>
<th>TIsmd</th>
<th>STsmd</th>
</tr>
</thead>
<tbody>
<tr>
<td>CiS</td>
<td>100%</td>
<td>100%</td>
<td>100%</td>
<td>100%</td>
<td>100%</td>
</tr>
<tr>
<td>IRST</td>
<td>90%</td>
<td>72%</td>
<td>100%</td>
<td>63%</td>
<td>100%</td>
</tr>
</tbody>
</table>

⇒ Again we need more statistics to estimate the figures with smaller errors
The currents for CiS sensors at 50V and 150V points. A couple of tiles broke before 150V point and did not enter the second plot.
The currents for IRST sensors at 50V and 150V points. The sensors draw quite high currents...
Summary

• The yield of CiS tiles with small dot grid having $V_{bd} > 40V$ is $\sim 100\%$. It reaches $\sim 75\%$ for $V_{bd} > 150V$. The single-chips have yield of $\sim 100\%$. From naive prob. calculations $(0.75)^{1/16} = 0.98 \ldots$

• The yield of IRST tiles with small dot grid having $V_{bd} > 40V$ is $\sim 63\%$ while the single-chip partners have practically $\sim 100\%$ yield. For $V_{bd} > 150V$ the yield of IRST “small dot” tiles amounts $\sim 17\%$.

• IRST sensors have systematically lower breakdown voltages than CiS ones.

• Everywhere the tiles perform worse than there single-chip partners.
• The currents are consistent with the quality expectations of the sensors

• need larger statistics to be collected from other labs

• provided IRST just started to gain the experience with p-spray technology, there results look as promising as from CiS. We need more wafers from them to investigate the situation.

The End