Report from the Vertexing and Tracking Session
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Introduction (Science Drivers)

Vertexing and tracking detectors are needed for the realization of several of the P5 Science Drivers for compelling lines of inquiry. These detectors will be especially central to: Driver 1, Use the Higgs boson as a new tool for discovery; Driver 2, Pursue the physics associated with neutrino mass; and Driver 5, Explore the unknown. Given that the ATLAS and CMS HL-LHC tracking systems will require 200 m^2 of silicon, LHC experiments are a primary motivation for tracking technology development at this time; frontier work is ongoing as well on pixel readout and pattern reconstruction algorithms for DUNE.

Critical Needs (Findings)

- Enabling production of sensors and readout from 8" silicon wafers could reduce costs and reduce the number of components needed to tile a detector. Present 8" wafers being developed by several vendors require specialized equipment to thin them and handle them after thinning.
- Significant progress has been made in optimizing 3D silicon sensors for HL-LHC conditions. This technology is mature. Recent research has aimed at raising the reverse breakdown voltage and exploring the role of surface damage in breakdown.
- Diamond detectors have been used in luminosity monitors for measurements of precision better than 1%. 3D-geometry diamond sensors have been fabricated in polycrystalline and single crystal materials.
- HV-CMOS monolithic active sensor technology continues to mature. The design of the CHESS2 front end readout of multisegmented sensors is underway. This full reticle demonstrator strip sensor fully encodes hits for all the pixels and is fully synchronous at 40 MHz.
- Ultra-fast silicon detectors, based on low gain avalanche detectors, provide good position and time resolution, can take high rates, and can be arranged to form large arrays and cover large areas. Detectors fabricated to date show stable operation with gain around 20 and good gain uniformity.
- Progress toward the RD53 common pixel readout design continues. As part of this, a CMS pixel readout (FCP130) is under development with a goal to test a synchronous front end with asynchronous output data flow for architecture at 130nm prior to realization in 65nm. The IFCP65 device will adapt this to 65nm.
- A self-adjusting pixel threshold mechanism is under development which, referenced to noise hit rate, automatically adjusts for SEUs and changes in transistor characteristics. Digital and analog designs are possible, and digital is being pursued first, for compatibility with traditional calibration.

- Ultralight detector thermostructures are under study, including a composite sandwich with a three-layer laminate, foam core, and titanium cooling tube, based on evaporative carbon dioxide at -35C.

Future Directions (Comments, Recommendations, Grand Challenges)

- 8" wafers will allow experimenters to 3D-bond full sensors with proper topology to IC wafers, integrating multiple layers, providing better power distribution and connectivity, reducing interconnect capacitance, and resulting in complex electronics without expensive process nodes.
- Improved understanding and control of surface damage in 3D silicon sensors will extend the reliability and applicability of this technology.
- New techniques to improve the performance and production of 3D polycrystalline diamond pixels should lead to more efficient column creation and optimized column penetration depth and cell layout.
- Continued development of CMOS technology will provide engineering and detection advantages including reduction of the number of wirebonds, reduction of detector capacitance, and reduction of material budget.
- Continued studies of the effects of radiation on ultra-thin UFSDs/LGADs should lead to optimized designs for capacitance and cooling. An optimized VLSI readout for these should provide further improvement in signal to noise ratio. A fine pitch pixel version will allow much better position measurement while maintaining timing accuracy.
- The RD53A project must demonstrate small pixels, low in-time effective threshold, 4b charge at high rate, high hit rate, time walk below 25ns, a specified digital buffering/processing rate, a trigger rate of 1 MHz, acceptable power consumption, serial powering, high radiation tolerance, and compatibility with bump bonded sensors.
- Threshold stability over time is a challenge in HEP experiments and will become worse in the high fluence HL-LHC condition which promotes detuning; this motivates development of an SEU-immune self-tuned pixel chip architecture.
- Further mass reduction to ultralight detector thermostuctures may be achieved through further reduced laminate areal density, decreased foam density, and decreased adhesive mass. A variety of compensating options to offset loss in thermal conductivity remain to be studied.